Polytypic heterojunctions for wide bandgap semiconductor materials

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Abstract

The bonding of crystallic semiconductor structures for getting polytypic heterojunctions on the basis of wide band gap semiconductor materials has considerably increased. The direct wafer bonding technology for the creation of polytypic heterojunctions (e.g. silicon carbide polytypes like 4H-SiC, 6H-SiC, 3C-SiC) gives an advantage in obtaining heterojunctions on the basis of different polytypes improves the electrical and physical properties of devices without lattice mismatch problems. The bonding of SiC wafers is an extremely challenging process even under ideal surface conditions. The hardness and inertness of SiC renders possesses a huge influence for surface preparation. Such parameters as roughness, flatness, waviness, and an extremely important aspect like cleanliness of surfaces have to be tightly controlled.

This paper shows a state-of-the-art-today's situation: the physical background and surface preparation problems before the direct bonding; the technological possibilities and possible practical solutions.
Keywords: silicon carbide, polytypic heterojunctions, wafer bonding/diffusion welding, surface preparation.

1 Introduction

Silicon carbide (SiC) was discovered in 1890 during an experiment on the synthesis of diamonds. Now more than 200 crystalline modifications are known. SiC has a large family of similar crystalline structures are called polytypes. The differences among the existing polytypes are based on orientation sequences. SiC layers can form many crystal structures by different ways of stacking the layers on


WIT Transactions on Engineering Sciences, Vol 90, © 2015 WIT Press
www.witpress.com, ISSN 1743-3533 (on-line)
doi:10.2495/MC150251

top of each other. The variations of the same chemical compound that are identical in two dimensions and differ in the third, which can be viewed as layers stacked in a certain sequence.

The most common polytypes of SiC for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. The cubic 3C is commonly referred to be as beta silicon carbide (β-SiC), which has the zinc blende crystal structure (similar to diamond), and is formed at temperatures below 1700°C. The rest two polytypes are referred to be as alpha silicon carbide (α-SiC) having a hexagonal crystal structure (mainly 6H-SiC), which is a wurtzite structure, and is formed at temperatures over 1700°C.

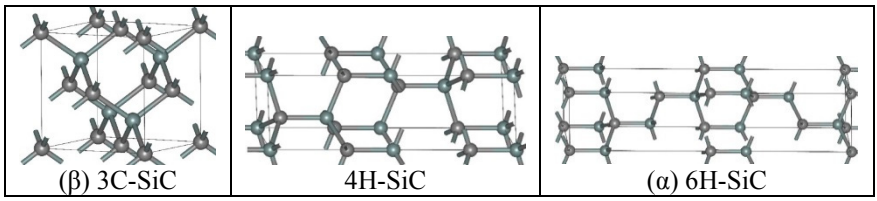

Figure 1: Structure of major SiC polytypes (figure copied from http://en.wikipedia.org/wiki/Silicon_carbide (05.12.2014).

It has been found that silicon carbide polytypes are semiconductors with an indirect band structure. The band gap width strongly depends on the polytype and varies from 2.39eV for 3C-SiC to 3.26eV for 4H-SiC. Thus, the difference in the band gap of cubic and hexagonal polytypes of SiC is about 0.87eV, which make it a very interesting for many electronic applications [1].

Bonding of SiC wafers is an extremely difficult task, because the stability of SiC surfaces at elevated temperatures typical for fusion bonding makes direct SiC-to-SiC bonding almost impossible, even an ideal condition. Surface passivation is a crucial issue in successful SiC device technology. Research has shown that achieving a level of surface roughness for large area bonding is also very difficult by reason of hardness and inertness of SiC and renders most chemical and chemical-mechanical polishing processes ineffective. It is worth noting that SiC wafer bonding could be used to fabricate heterostructures which cannot be obtained by conventional epitaxial growth because of lattice mismatch. Another relevant point is surface condition as roughness, contaminations which make the bonding process more challenging. In this case, high temperature combined with applied stress, is an effective route for a successful process [2, 3].

2 Practical application fields for polytypic heterojunctions

Direct wafer bonding is a promising process for manufacturing heterostructures based on the combinations of SiC wafers of various polytypes. Assuming that direct wafer bonding technology could be used for polytypic heterojunctions of silicon carbide (4H-SiC, 6H-SiC, 3C-SiC), it gives an advantage in obtaining heterojunctions by using wafers with different polytypes, electrical and physical properties without lattice mismatch problems, which cannot be made by

conventional epitaxial growth. The electrical parameters of individual SiC wafers can be controlled before direct wafer bonding.

Among others, the promising research area in modern semiconductor technology is formation of two-dimensional electron gases (2DEG) in polytypic SiC heterojunctions, which could be found the practical applications in high electron mobility transistors (HEMTs), heterojunction field effect transistors (HFETs) and heterojunction bipolar transistors (HBTs). The formation of 2DEG in polytypic SiC heterostructures gives strong carrier confinement, high carrier sheet density, and enhanced mobility. SiC polytypes form heterostructures consisting of chemically identical, but structurally different constituents. It is worth noting that formation of two-dimensional electron gases 2DEGs at polytypic hexagonal/cubic SiC heterojunctions 4H/3C SiC and 6H/3C SiC has been investigated by numerical self-consistent solutions of the Schrödinger and Poisson equations.

Research has shown [4] that 4H/3C SiC heterostructures becomes a promising candidate, but the 6H/3C structure is less promising for application in HEMTs. The 2DEG sheet densities in 4H/3C SiC heterostructures are substantially higher and less sensitive to variations of the barrier thickness in comparison to $Al_{0.3}Ga_{0.7}N/GaN$ structures, which is the competitor for SiC polytypic heterojunction solutions today. The doping of the barrier layer yields a noticeable enhancement of the 2DEG density only for the 4H/3C SiC structure, e.g. [4–7].

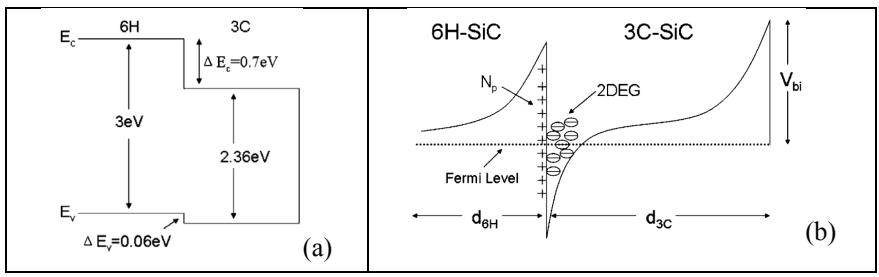

Figure 2: Polytypic heterojunctions (e.g. [8]). (a) Band diagram for 6H-SiC and 3C-SiC; (b) Schematic illustrating the electrostatics of the 3C-/6H-SiC heterostructure at equilibrium, where N_p is the positive polarization charge at the C-face of SiC.

SiC is a material of choice for high temperature and high power applications due to its superior material as well as electrical properties over Si and GaAs and the availability of different polytypes in SiC. 4H-SiC BJTs have been extensively studied in the recent years however their main drawback is the low current gain e.g. [1, 2].

The heterojunction bipolar transistor (HBT) is a type of bipolar junction transistor (BJT), which uses different SiC polytypes for creation heterojunction between the emitter and base regions. The emitter efficiency HBT is improved because the injection of holes from the base into the emitter region is limited since the potential barrier in the valence band higher than in the conduction band.

Potential 6H-SiC/3C-SiC HBT can handle signals of very high frequencies, up to several hundred GHz. It is commonly used in modern ultrafast circuits, mostly radio-frequency (RF) systems, in high power efficiency, such as RF power amplifiers in cellular phones. A possible design of 4H-SiC/ 6H-SiC n-p-n HBT is described for example in [8].

The bonding of SiC wafers can be divided into three categories: bonding with a conducting interlayer, an insulating interlayer and without an intermediate layer (direct bonding). Direct bonding is a wafer bonding process without any additional intermediate layers. All of these categories are used extensively in the microelectronics industry. It has been found that bonding SiC–SiC with titanium (Ti) interlayers (physical vapor deposition (PVD) and pure metallic foils), titanium aluminate (TiAl) and silicone resin have good bonding results but unfortunately it does not alloy to implement heterojunction, e.g. [9–12].

3 Physical background, surface preparation, technological possibilities and practical solutions

The procedural steps of the direct bonding process of wafers any surface is divided into wafer preprocessing or surface preparation; pre-bonding at room temperature; and annealing at elevated temperatures. Bonding process is based on the chemical bonds between the two atomically smooth and flat surfaces which adhere to each other by annealing at elevated temperatures with applied stress. Bonding strength is a function of temperature and applied stress.

Direct bonding is performed in vacuum when three major types of surface forces can be presented as van der Waals forces, electrostatic forces, and short-range forces. Short-range forces become effective when the atoms of two contacted surfaces are within a very close distance (0.2 nm). Surface forces between the two wafers determine their adhesion upon initial contact. When electron clouds of the two atoms start overlapping each other is formed a bond, covalent bonds are prevalent in SiC. It is emphasized that requirements for the wafer surfaces as sufficiently clean, flat and smooth should be specified. The following parameters as micro-roughness, macroscopic surface roughness or waviness, wafer bow, surface contaminations have to be tightly controlled, and otherwise might introduce unbonded areas so called voids, i.e. interface bubbles.

The surface roughness should be close to the lattice constant value, about 0.3–0.5 nm. The surface roughness is a measurement of tool marks in terms of RMS (root mean square) which is measured with a relatively short sampling length and suppresses waviness. In this case, RMS roughness of up to about 0.5 nm can be tolerated (for room temperature bonding). Micro-roughness of the surface of a wafer can be measured by Atomic Force Microscopy (AFM). It allows a 3D profile of the surface. The microscope can run in following modes: contact, non-contact and tapping modes. Tapping mode AFM provides the best quality data for surface roughness determinations, offers higher lateral resolution on most samples (1 to 5 nm), relatively high scan speeds, less damage to soft samples imaged in the air and a minimum distortion in the image [8]. It is important to pay attention on macroscopic surface roughness (waviness) as well. For example the surface profile

is a value for the peak-to-valley waviness and should be approximately 3–6 μm for 12x22 mm^2 samples. It has been found that waviness is usually elastically accommodated during bonding. However, when it exceeds a certain critical value, the interface may not to be the bonded. To overcome the problem, the plasma etching can be used for reducing the waviness of wafers, as shown in [8]. All surface contamination, particles between two opposing surface wafers act as spacers strongly decrease intermolecular bonds. Size and coverage density leads to the creation of unbonded areas and even completely prevent bonding of wafers. It has been found (e.g. [8]) that the surface is covered with a very thin layer (several mono-layers in thickness), which does not strongly adhere to the surface and therefor for example by a nucleation of interfacial causes the contamination. In the same study [8] it has also been observed that metal contaminants are usually present at the surface in a small amount, that doesn't affect the adhesion of wafers. However, they may strongly affect the electrical properties of the interface and thus may be harmful for electronic applications of wafer bonding. SiO_2 is the native oxide of SiC which can trap metallic and organic contamination and thus also needs to be removed. In case of SiC, another unique phenomenon has been observed that the oxidation of SiC is a face terminated oxidation, means the both polar faces (Si and C face) have different oxidation rates. These oxidation rates are also depend on the crystal orientation of SiC and polytypes i.e. silicon carbide shows an anisotropic oxidation nature [13].

To obtain a high quality interface, one needs to remove all contamination before bonding. The cleaning processes used in modern semiconductor industry are compatible with wafer bonding. Removing surface contaminants and achievement required roughness can be performed by wet chemical and dry plasma reactive etching methods. The wet chemical cleaning procedure, which is generally used in Si-Technology, has been adopted for cleaning wafers SiC [14]. The RCA (Radio Corporation of America) clean or RCA activation is a standard set of wafer cleaning steps which need to be performed before high-temperature processing steps. It involves the following chemical processes performed in sequence as removal of the organic contaminants (organic clean + particle clean), removal of thin oxide layer, removal of ionic contamination. The final step in the RCA clean procedure is to dry the wafers. The RCA wet cleaning procedure is most frequently used in industry. It involves two steps: RCA1 and RCA2, e.g. [8, 15].

There are no known conventional wet chemicals that etch single-crystal SiC at room temperature. Dry etching techniques are used for most patterned etching of SiC for electronic devices and circuits. Reactive ion etching (RIE) of SiC in fluorinated plasmas is the most commonly employed process. The SiC RIE process can be implemented using standard RIE hardware and typical 4H- and 6H-SiC RIE etch rates of the order of hundreds of angstroms per minute. The SiC RIE processes are typically highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. While RIE etch rates are sufficient for many electronic applications, much higher SiC etch rates are necessary to carve features of the order of tens to hundreds of micrometers deep that are needed to realize advanced sensors, MEMS, and through-wafer holes useful for SiC RF devices. RIE of SiC

has been performed using SF_6/O_2 and SF_6/Ar gas. The gas ratios and etch rates have been evaluated, for example etch rates as high as 900Å/min using SF_6/Ar at a 10:40 sccm ratio. Research has shown that RIE of SiC with fluorine containing plasmas gives the fast etch rates of SiC up to 0.45 μm/min. The same etch rates were obtained for SiC in SF_6/O_2 mixture [16]. High-density plasma dry etching techniques such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) have been developed to meet the need for deep etching of SiC. Residue-free patterned etch rates exceeding a thousand angstroms a minute have been demonstrated, e.g. [17–19].

4 Problematic questions

Pre-bonding The wafers can be brought into contact in deionized water. Then, each sample is dried in a centrifuge and treated for 4h in air at temperature ~ 95–100°C under a load of ~0.5 kgf/cm^2. Finally, the wafers are subjected to a high-temperature treatment for 2h in air at 1250°C under the same load (~0.5 kgf/cm^2). Low temperature wafer bonding techniques for activation of SiC surfaces can be generally divided into two groups: wet chemical and dry physical methods (UV exposition, electron or ion beam, low pressure plasma treatment, etc.), e.g. [20]. Inclusion of particles or obstacles on the wafers as result of insufficient polishing can lead to unbonded areas between the wafers that are generally referred to as interface bubbles or simply bubbles or voids. The particle with a diameter of about 1μm causes a bubble with a lateral diameter of several mm. Provided using proper cleaning, a sufficiently high-quality cleanroom (class 10 or better) or other specifically designed equipment for wafer bonding interface bubbles caused by particles can be avoided. The micro-cleanroom is basically a spinner in which the two wafers are placed with the mirror-polished surfaces facing each other, separated by removable spacers [15].

Annealing SiC wafer direct bonding can be performed under a uniaxial stress of 20 MPa for a period of 15 hours in a temperature range of 800°C to 1100°C. Results reveal that at 20 MPa of applied stress, 6H-SiC wafers can be bonded at temperatures greater than 800°C. Complete bonding over the whole area of the specimen can be achieved at temperatures above 950°C. It is worth noting that an ability of SiC wafers to bond did not significantly depend on the mutual orientation of wafers [8]. Another relevant point is that has been demonstrated in [8] that a difference in crystallographic orientations of the two surfaces does not significantly influence the direct wafer bonding process, while still substantially determining the electrical properties of the interface. The key aspect of this argument is that roughness and coefficients of thermal expansion of various SiC polytypes have very close values and could be encouraging for wafer bonding between different polytypes of SiC. It has been found that in the case of 6H-SiC/6H-SiC, the bonded area covered almost 100% of the contact area.

Another interesting study [22] has been made using direct bonding of SiC wafers with a regular relief at the interface. There has been studied direct wafer bonding of two wafers, one smooth and another bearing an artificial microscopic relief. Selective reactive ion etching is used for forming a regular pattern of

grooves with a depth, width, and spacing of 10, 50, and 200 μm. Small damage, surface contamination, and roughness have been removed from the surface by polishing with diamond pastes, chemical treatment, and thermal oxidation followed by the selective removal of oxide. Research has shown that in the best samples, the bonded surface fraction reaches 85% of the total area.

Failures Wafer bonding failures can be characterized as unbonded areas, voids, insufficient bond strength, or electrical contact failures. There are several different characterization methods available, non - destructive methods as infrared imaging (IR), scanning acoustic microscopy (SAM), X-Ray topography and destructive methods as scanning electron microscopy (SEM), transmission electron microscopy (TEM), voids decoration and optical microscopy. Materials related bonding defects. These defects are related to either materials properties or materials surface preparation or materials damages related to inappropriate handling or prior process steps [22]. The existence of interface bubbles can be revealed by standard non-destructive detection methods such as infrared transmission, ultrasonic microscopy, X-ray topography, or the so-called magic mirror method, which optically detects small surface deflections of the bonded wafers caused by interface bubbles. In case of smaller feature sizes can be applied destructive methods of analysis such as interface etching and transmission electron microscopy (TEM) [22].

Characterization It is known nondestructive and destructive techniques for mechanical characterization of the bonding process. The most common techniques which could be implemented are a bond imaging, cross-sectional analysis, and bond-strength measurement. The imaging methods are nondestructive and can be used as in-process monitors, while the cross-sectional analysis and bond-strength measurements are destructive and require control wafers for characterization. The dominant methods for imaging a bonded pair of wafers are an infrared transmission, ultrasonic, and X-ray topography.

Scanning acoustic microscopy is a powerful nondestructive method for interface analysis. It offers high spatial resolution of up to 10 mm (compared to that of about 100-500 mm for an infrared system) and is applicable to any combination of bonded materials. Scanning acoustic microscope generates images by scanning a focused spot of ultrasound over the interface of the specimen and detecting a reflected signal. Cross-sectional analysis can be performed at the bonded interface by cleaving the sample. Scanning electron microscope (SEM) and transmission electron microscope (TEM) techniques are used to image the bonded interface at a sub micrometer scale. TEM is the method that affords a detailed characterization of the bonded interface at the atomic level. Spatial resolution of modern microscopes reaches down to 0.15 nm [8]. The bond strength has been characterized by a number of techniques as pressure burst tests, tensile/shears test and knife-edge, or double cantilever technique [23].

5 Conclusion

The question number one is how to increase bonded surface area by reducing time and temperature annealing. The second critical question is the pre-bonding surface

preparation contacting two mirror-polished wafers for bonding to avoid particles between the wafers. The third problem concludes from the pre-bonded technology application to get the reliable and repeatable result throughout the entire bonding process. It is clear from above that using interlayer's metal or silicon nano-layers for bonding two SiC–SiC wafers could be very interesting.

The effect of dissolving of the silicon film on a SiC surface seems to be best practice and the key issue connecting the SiC wafers with different polytypes to form the polytypic heterojunctions. Bonding of SiC wafers is an extremely difficult task, because the stability of SiC surfaces at elevated temperatures typical for fusion bonding makes direct SiC-to-SiC bonding almost impossible, for instance by uniaxial stress of 20 MPa for a period of 15 hours in a temperature range of 800°C to 1100°C. The surface condition as roughness about 0.5 nm, all surface contamination, particles between surfaces is made the bonding process an incredible challenging. A micro-cleanroom allows for fabrication of particle-free wafer bonding. Using nano-layer Si as bonding interlayer between SiC wafers it could be the key to form polytypic heterojunctions.

Today we are in the situation where the practical bonding steps are foreseen. We plan to use Physical Vapor Deposition (PVD) for coating of silicon as an internal layer (nano-layer) for bonding two SiC–SiC wafers. The thickness of nano-layer, which provides bonding of two SiC–SiC wafers, should be controlled so that any influence on electrical parameters for polytypic heterojunctions will take place. Dry Reactive Ion Etching (RIE) in fluorinated plasmas have been planned to use for pre-bonding surface preparation.

Acknowledgements

The authors wish to thank the Estonian Research Council who supported this research under research projects ETF8592 and IUT19-11, and the Foundation Archimedes through the Centre of Excellence CEBE (TK05U01) for supporting technology oriented scientific projects in Estonia.

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