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Boundary element methods for capacitance and substrate resistance calculations in a VLSI layout verification package

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ABSTRACT

In this paper we describe the application of the Boundary Element Method to the layout verification of VLSI Designs. We describe the methods for the calculation of interconnection capacitances and substrate resistances with the use of problem specific Green's functions. Emphasis is on computational efficiency and practical accuracy. The methods are implemented in the layout extractor Space (van der Meijs [1]).

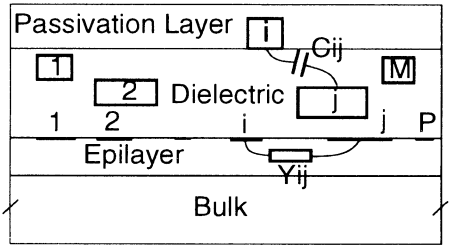
INTRODUCTION

Designers of modern VLSI circuits rely heavily on layout-to-circuit extractors, which translate a chip layout into an equivalent network suitable for electrical verification of their layouts. Because of the growing influence of parasitic elements, such extractors must be able to model (extract) more and more parasitic phenomena. Parasitic capacitances and coupling between different components via the substrate of the chip are severe problems, see e.g. Bakoglu [2] and Kup [3]. We describe Boundary Element Methods for the calculation of interconnection capacitances and substrate resistances for the layout-to-circuit extractor Space (van der Meijs [1]). These components are indicated in Figure 1. We do not attempt to solve a *field* problem for a given set of boundary conditions. Instead we want to obtain a *circuit model* for the given physical situation. In particular we seek the capacitance matrix C_s for the interconnect and the indefinite admittance matrix Y for the substrate.

Boundary Element Formulation

The problems mentioned above are generally described by the equation

$$\nabla(K\nabla u) = 0 \qquad \text{on a domain } \Omega. \tag{1}$$



- dielectric, containing M conductors:
  passivation, silicon nitride, $\epsilon_r = 7.5$.
  dielectric, silicon oxide, $\epsilon_r = 3.9$.
- silicon with P contacts on the boundary:
  epi-layer, low-doped, $\rho = 15\ \Omega$cm.
  bulk, high-doped, $\rho = 0.05\ \Omega$cm.

Figure 1: *Cross section of a chip.*

where u denotes the potential and K is a parameter of the medium. For constant K this equation reduces to the Laplace equation.

For the capacitance problem the domain is the semi-infinite layered half-space above the silicon. K is the permittivity (ϵ) of the domain. The domain contains M conductors with inhomogeneous Dirichlet conditions. Homogeneous Dirichlet conditions hold at the groundplane and infinity. The unknowns are the charges on the conductors.

For the resistance problem the domain is a cuboid with conductivity $K = 1/\rho$. The substrate is contacted by P contacts with inhomogeneous Dirichlet conditions. Homogeneous Neumann conditions hold on the remainder of the boundary. The unknowns are the currents through the contacts.

The above problems may be rewritten as a boundary integral equation Brebbia [4]

$$\alpha u + \int_{\Gamma_1} \overline{u} \frac{\partial u^*}{\partial n} d\Gamma + \int_{\Gamma_2} u \frac{\partial u^*}{\partial n} d\Gamma = \int_{\Gamma_1} \frac{\partial u}{\partial n} u^* d\Gamma + \int_{\Gamma_2} \overline{\left(\frac{\partial u}{\partial n}\right)} u^* d\Gamma \qquad (2)$$

where overlined quantities are prescribed by boundary conditions and u^* is a fundamental solution or the (free space) Green's function. Γ_1 denotes the part of the boundary with Dirichlet conditions and Γ_2 denotes the part of the boundary with Neumann conditions. Green's function satisfies

$$\nabla^2 u^*(\vec{x}; \vec{x_s}) = -\delta(\vec{x} - \vec{x_s}) \qquad (3)$$

and can be interpreted as the potential caused by a unit point charge at $\vec{x_s}$. We do not use the free space Green's function, but Green's functions which are tailored by boundary conditions additional to Equation (3) for the particular problems. The result is such that only the third integral in Equation (2) remains. The derivation of the Green's functions will be discussed in the next sections. The boundary Γ_1 is discretized into N elements, piecewise constant shape functions are assumed for the unknowns and using the collocation method we obtain

$$\alpha u_i = \sum_{j=1}^{N} \left.\frac{\partial u}{\partial n}\right|_{\text{element}_j} \int_{\Gamma_{1,j}} G(\vec{x_i}; \vec{x_j}) d\Gamma_j, \qquad i = 1, 2, 3, ..., N \qquad (4)$$

or in matrixform $U = GQ$. Here U is the vector of N element potentials and Q is the vector of N unknowns on the elements. For these problems it can be shown that $\alpha = 1$. The elastance matrix G now describes the influence between each pair of boundary elements. By defining an incidence matrix F, which relates the element potentials U to the known conductor potential vector V by $U = FV$ and the vector of element unknowns Q to the conductor unknowns X by $X = F^T Q$ we easily find the desired model relation

$$X = F^T G^{-1} F V = MV \tag{5}$$

3D INTERCONNECTION CAPACITANCE CALCULATIONS

For the case of 3-dimensional capacitance calculations, $C_s = M$ is the desired capacitance model. The domain is treated as a semi-inifinite stratified halfspace, i.e. it consists of layers of constant permittivity and the substrate acts as a groundplane. This is justified for the frequencies of interest ($<$ 1Ghz). The discussion below will be necessarily brief, see van der Meijs [5] and van Genderen [6] for more detail and additional references.

Green's Function and Model Reduction

We write the Green's function for this problem as $G(\vec{x}; \vec{x_s}) = u^* + u^+$, where u^* is the free space solution. u^+ satisfies Equation (1), with the boundary conditions specified in the previous section. Additionally, it satisfies the conditions that the potential and normal derivative of the electric displacement are continuous across the dielectric interfaces. Since the physical situation is rotationally symmetric around $\vec{x_s}$, we can write Equation (1) in cylindrical coordinates with the z-axis through $\vec{x_s}$ and the origin at the groundplane. By separation of variables we obtain $u^+ = Z(z; z_s)R(r)$, where Z satisfies the hyperbolic (second order) ODE and R satisfies the Bessel equation of order zero. When this system is solved, the solution containing the Bessel function of the second kind is rejected because of the boundary conditions. The Green's function can then be written as a linear combination of the independent solutions as:

$$G = u^* + \int_{m=0}^{\infty} \left(H_1(m) e^{m(z-z_s)} + H_2(m) e^{m(z_s-z)} \right) J_0(mr) dr \tag{6}$$

H_1 and H_2 are determined by the boundary and additional conditions. Standard numerical procedures then lead to the following result:

$$G(\vec{x}; \vec{x_s}) = \sum_{n=0}^{\infty} \frac{s_n}{\sqrt{r^2 + (z - z_n)^2}} \tag{7}$$

Here, the s_n and z_n can be interpreted as the image coefficients and positions, respectively (Zauderer [8]). In particular, $s_0 = 1/(4\pi K)$ and $z_0 = z_s$, so that the 0'th term is the free-space solution u^*. Equation (4) can be integrated either analytically or numerically. Thus, C_s can be calculated by Equation (5).

However, C_s is a full matrix which specifies a capacitance between every pair of conductors. For our application, this corresponds to a circuit that contains too much irrelevant detail since conductors that are far apart have a negligible (although non-zero) capacitance. Moreover, computational complexity would restrict the applicability of the method to situations without practical significance.

Therefore, we calculate a *reduced* capacitance model with the so-called hierarchical Schur algorithm. This algorithm produces an approximate positive definite sparse inverse G_{SI}^{-1} for a positive definite matrix G that is specified on a double band S. G_{SI}^{-1} has zeros on the complement of S and is the exact inverse of the so-called maximum entropy extension of a matrix G' that is close to G. It has been shown, see Nelis [7], that under certain conditions G_{SI}^{-1} is an optimal reduced model.

Thus, we compute a sparse approximation G_{SI}^{-1} of G^{-1}, thereby in effect ignoring small capacitances between conductors that are physically 'far' from each other. The distance w, above which capacitances are ignored, is a parameter of the method. This allows to trade detail of the model against computation time.

The algorithm requires $O(Nb^2)$ operations, where N is the number of boundary elements and b is the average number of non-zero entries on a row of G_{SI}^{-1}. This latter quantity is determined by the average number of nearby elements, which does not depend on the problem size but only on the window size w and the mesh granularity. Consequently, the running time is in practice proportional to the size of the problem.

Implementation and Results

The method as described above is implemented in an IC verification program called Space (van der Meijs [1]). From a layout description of a chip, Space produces a circuit netlist that contains the interconnect capacitances as well as the active devices and interconnect resistances.

Space incorporates all steps of the method in a single program that performs one single pass over the input data. It reads a layout database and a file containing the relevant technological data, and defines a window that is swept over the layout. Within the window, the mesh is created, the collocation integral is computed for all pairs of boundary elements within the window, the resulting (partially specified) elastance matrix is inverted on the fly, and the approximate inverse is multiplied by the the incidence matrix. The result is merged with the network of active devices and interconnect resistances, and written to a netlist database. This netlist is ready for simulation, e.g. with Spice (Quarles [10]).

To illustrate the efficiency of the program, consider a layout consisting of two crossing busses of 5 wires each, see Figure 2. The lower conductors are numbered 1-5 and the upper conductors are numbered 6-10. The thickness and width of the conductors, as well as the horizontal and vertical separations are all 1μm. The medium consists of a single semi-infinite dielectric layer with a

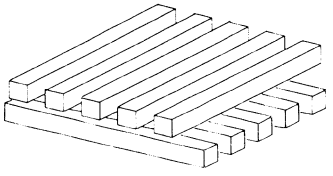


Figure 2: *Crossing-bus example layout.*

Table 1: *Results as a function of the window size, on an HP 9000/720.*

w	time	mem	capacitances (10^{-18}F)					
(μm)	(sec)	(Mbyte)	$C_{1\,\mathrm{gnd}}$	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}
11	144.5	14.74	453.1	586.6	44.3	17.9	12.3	144.6
5	83.2	4.14	462.5	585.0	43.3	17.2	11.9	143.9
4	47.8	2.10	476.0	584.0	43.0	21.3		143.4
3	26.8	0.78	499.0	582.6	5.0			142.9
2	12.5	0.32	554.2	599.3				141.4
1	3.6	0.14	645.4	490.8				139.9

relative permittivity of 3.9 (SiO_2). The boundary element mesh that is created by Space consists of 460 elements of $1\mu\mathrm{m} \times 1\mu\mathrm{m}$.

The results of extracting this layout when the window size w is varied, are shown in Table 1. For $w = 11\mu\mathrm{m}$, they correspond to an exact inversion of the elastance matrix. Note that when a capacitance C_{ij} vanishes, the corresponding ground capacitance $C_{i\,\mathrm{gnd}}$ increases so that the total capacitance of a conductor changes very little. This will ensure accurate delay simulation, at the cost of less crosstalk detail. Small values of w thus give acceptable capacitance models, however, with much reduced memory use and CPU times.

Further results, including comparison to results obtained with other programs, can be found in van der Meijs [5].

3D SUBSTRATE RESISTANCE CALCULATIONS

The substrate of a VLSI chip may be seen as a multi-terminal distributed resistance network between the contacts on the boundary of the substrate. These contacts may be explicitly designed substrate contacts and e.g. substrate terminals of (active) devices such as MOSFETs. $Y = M$ is the desired indefinite admittance matrix of this network.

Theory

We specify the Green's function by demanding homogeneous Neumann boundary conditions on Γ_1 *and* Γ_2 for the fundamental solution. The homogeneous Neumann conditions and the divergence theorem require that the volume integral of the right-hand-side of Equation (3) equals 0. Therefore this equation

has to be modified to

$$\nabla^2 G(\vec{x};\vec{x_s}) = -\delta(\vec{x}-\vec{x_s}) + \frac{1}{V_\Omega} \tag{8}$$

The last term can be seen as a sink, distributed over the volume V_Ω, with a strength equal to the source at $\vec{x_s}$. The Green's function is obtained by the operator technique (Zauderer [8]). The 3D function is expressed as a series expansion in a basis of 2D eigenfunctions. For symmetry reasons we demand that the function must be independent of the choice for the base directions (in this case x and y). Then the Green's function is given by:

$$G(\vec{x};\vec{x_s}) = C + \frac{4}{\pi}\sum_{m,n=0}^{\infty} \gamma_{mn} \frac{T_{mn}\cos\left(\frac{m\pi x}{L}\right)\cos\left(\frac{m\pi x_0}{L}\right)\cos\left(\frac{n\pi y}{W}\right)\cos\left(\frac{n\pi y_0}{W}\right)}{\sqrt{m^2W^2+n^2L^2}\sinh\left(\sqrt{\lambda_{mn}}H\right)}$$

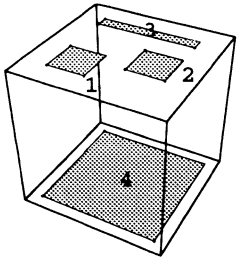
$$C = \begin{cases} \frac{(z^2+z_s^2)}{2LWH} - \frac{z_s}{LW} \\ \frac{(z^2+z_s^2)}{2LWH} - \frac{z}{LW} \end{cases} + \frac{H}{3LW}, \qquad \gamma_{mn} = \begin{cases} 0 & m=n=0 \\ 0.5 & m=0 \otimes n=0 \\ 1 & m,n=1,2,\ldots \end{cases} \tag{9}$$

$$T_{mn} = \begin{cases} \cosh\left[\sqrt{\lambda_{mn}}\,(H-z_0)\right]\cosh\left[\sqrt{\lambda_{mn}}z\right], & 0<z<z_0 \\ \cosh\left[\sqrt{\lambda_{mn}}z_0\right]\cosh\left[\sqrt{\lambda_{mn}}\,(H-z)\right], & z_0<z<H. \end{cases}$$

The sink term in Equation (8) causes a new constant (unknown) term Ψ to appear in Equation (4). This term is the average potential over the domain. The normal derivative of the potential is related to the current density through the contacts by the local form of Ohm's law. To complete the set of equations, we use the Kirchhoff current law, which states that the sum of all terminal currents equals 0. Thus the indefinite admittance matrix of the substrate is given by $Y = F^T G_+^{-1} F$. Here G_+ results from the matrix $-(1/K)G$ augmented such that Ψ is the $(N+1)^{\text{th}}$ unknown and the Kirchhoff current law is the $(N+1)^{\text{th}}$ equation and multiplying by a diagonal matrix with the area of the elements as entries. The incidence matrices are modified appropriately.

Results

The accuracy of the method in 2D situations has been established in Smedes [9]. Here we will focus on 3D results. The structure in Figure 3 is calculated without and with the bottom contact. The resulting admittance matrices are shown as G2a and G2b, respectively. Matrix G2a can be obtained from G2b by Gaussian elimination. We verified that this relation holds for the numerical results, with a maximum error of 0.3%. From the matrices one can see that a substrate contact at the backside of a chip decreases the coupling between points at the surface. In effect, it acts as a sink for the disturbances injected into the substrate.

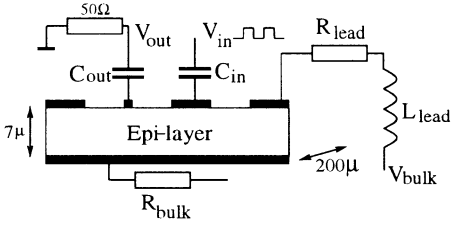


$$G2a = \begin{pmatrix} 4.88081 & -2.4078 & -2.47302 \\ -2.40166 & 5.57079 & -3.16914 \\ -2.47916 & -3.163 & 5.64215 \end{pmatrix}$$

$$G2b = \begin{pmatrix} 5.82148 & -1.51848 & -1.37216 & -2.93084 \\ -1.51529 & 6.4316 & -2.11119 & -2.80512 \\ -1.37397 & -2.0973 & 6.98414 & -3.51287 \\ -2.93223 & -2.81582 & -3.50079 & 9.24884 \end{pmatrix}$$

Figure 3: *3D structure with calculated admittance matrices.*

Figure 4 shows a structure which is typical for actual design problems. The structure represents a 15 Ωcm epi-layer on a good conducting substrate ($\rho = 0.05$ Ωcm). The outer top contacts are substrate contacts. Of the inner contacts the right one represents the output (drain implant) of a digital oscillator and the left one a sensitive node in an analog circuit. All top contacts are 50μm wide and 50μm separated, except for the output contact, which is 10μm wide. Figure 5 shows results obtained by simulation of the calculated substrate admittance matrix together with the external components with SPICE (Quarles [10]). The simulations are repeated with one or more of the substrate contacts in use. It is clearly seen that the addition of substrate contacts decreases the parasitic coupling.



Simulation data:

$V_{in} = 5V$	$f_{Vin} = 100MHz$
$V_{bulk} = -5V$	$R_{bulk} = 2.5\Omega$
$C_{in} = 0.2pF$	$C_{out} = 0.1pF$
$R_{lead} = 2\Omega$	$L_{lead} = 10nH$

Figure 4: *Example structure for substrate resistance calculations.*

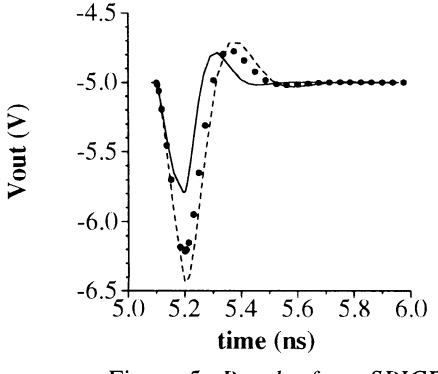


Figure 5: *Results from SPICE of structure from Figure 4.*

CONCLUSIONS

This paper describes Boundary Element Methods applied to the calculation of interconnection capacitances and substrate resistances for the verification of VLSI designs. The methods use Green's functions tailored to the specific problem, such that a simple integral formulation remains. This formulation is transformed into the desired capacitance and admittance matrices. The approximative inversion of the elastance matrix can be done with linear time complexity with the Schur algorithm. We showed the applicability of the methods by several examples.

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